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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,496	10/24/2003	Leonard W. Helmer JR.	POU920030106US1	1872

23334 7590 10/18/2007

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EXAMINER	
BURGESS, BARBARA N	
ART UNIT	**PAPER NUMBER**
2157	

MAIL DATE	DELIVERY MODE
10/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/692,496	HELMER ET AL.	
	Examiner	Art Unit	
	Barbara N. Burgess	2157	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10-24-03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10-24-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on October 24, 2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

2. Claim 1 objected to because of the following informalities: line 7 states "speculatively pre-defined *the* destination". Examiner understands this to mean "speculatively pre-defined destination" until further clarification. Appropriate correction is required.

3. Claim 1 objected to because of the following informalities: Claim 1 recites the limitation "the pre-defined destination" in line 9. In order to clarify the claim language, should "the pre-defined destination" read ----the speculatively pre-defined destination---- ? Appropriate correction is required.

4. Claim 2 is objected to because of the following informalities: Claim 2 recites the limitation "the pre-defined destination" in lines 14-15. In order to clarify the claim language, should "the pre-defined destination" read ----the speculatively pre-defined destination----? Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 1 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has not clearly defined what a "speculatively pre-defined destination" in line 1 is. However, the Examiner will interpret the "speculatively pre-defined destination" to be a defined destination until further clarification from the Applicant.

7. Claim 2 recites the limitation "the first data element" in lines 11-13. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 3 recites the limitation "the first data element" in lines 17-18. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 4 recites the limitation "the first data element" in line 2. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 8 recites the limitation "the fast data packet transmitter" in line 6. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 101

11. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

12. Claims 14-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter reciting "a signal bearing medium". On pages 6,

9, 23, and 25-26 of the specification, Applicant has provided evidence that Applicant intends the medium to include signals, as such the claim is drawn to a form of energy. Energy is not one of the four categories of invention and therefore these claims are not statutory. Energy is not a series of steps or acts and thus is not a process. Energy is not a physical article or object and as such is not a machine or manufacture. Energy is not combination of substances and therefore not a composition of matter.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

14. Claims 1-2, 4-6, 8-9, 11-15, 17-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Goldenberg et al. (hereinafter "Golden", US Patent Publication 2004/0034718 A1).

As per claim 1, Golden discloses a method, in a computer node, for transferring a data message, the method comprising:

- transferring a first data packet to a speculatively pre-defined destination (paragraphs [0010, 0013, 0019, 0045, 0049], Golden teaches writing (transferring) data (first data packet) from a received message to a specific memory location (destination);
- loading a packet descriptor into a communications adapter, wherein the loading is concurrent with the transferring and the packet descriptor identifies the speculatively pre- defined the destination (paragraphs [0008-0010, 0017, 0019, 0045], Golden teaches placing (loading) descriptors in the network adapter's cache. The descriptors are used to identify the memory address to which data should be written. The memory address corresponds to a memory location at a computing device. The adapter transfers the message data to the system memory location. The next descriptor is prefetched (loaded). Transferring the packet and prefetching (loading) the next descriptor is done in this manner to reduce latency. Without waiting, the adapter is able to increase its rate of processing messages under conditions of heavy, bursty traffic. Once data is being transferred to the memory location, the processing is complete and the network adapter is at that point able to prefetch (load) the next descriptor. Therefore, Golden implicitly discloses loading and transferring being done concurrently);
- transferring, in dependence upon the packet descriptor, a second data element to the pre-defined destination (paragraphs [0009, 0015, 0047, 0049], Golden teaches transferring the next incoming message (second data element) according to information contained in the pre-fetched descriptor. Subsequent packets (second data element) are sent to memory locations (destination) specified by the

descriptor).

As per claim 2, Golden discloses the method according to claim 1, wherein the transferring of the first data element and the transferring of the second data element comprises loading the first data element and the second data element into a fast data queue, wherein the fast data queue only queues data elements for transmission to the pre-defined destination (paragraphs [0004, 0006, 0033, 0037], Figure 2, According to Applicant's specification, an exemplary fast transmission queue structure has two queues: the fast data transmission queue and the fast descriptor queue. However, alternative embodiments operate with a single queue to queue entire data packets (pages 14-15). Golden teaches queue pair (QP) (fast data queue) having a send work queue and a receive work queue. Work requests having work elements (data elements) are placed in the appropriate queue. The receive queue comprise one or more descriptors indicating the memory location to which the data is to be written).

As per claim 4, Golden discloses the method according to claim 1, wherein the loading further comprises configuring, concurrently with the transferring of the first data element, the communications adapter for the transferring of the second data element (paragraphs [0008-0010, 0049, 0060], According to Applicant's specification, pre-fetching causes the network adapter to pre-fetch the descriptor from the fast descriptor queue to begin configuration for transmission of the next data element (page 18). Golden teaches fetching (loading) the next work item from the receive queue and writing

(transferring) data to the location specified by the work item. Once these operations complete, the adapter can pre-fetch the next work item (descriptor) for the next message (element). This is configuration for transmission of the next data element. The next descriptor is prefetched (loaded). Transferring the packet and prefetching (loading) the next descriptor is done in this manner to reduce latency. Without waiting, the adapter is able to increase its rate of processing messages under conditions of heavy, bursty traffic. Once data is being transferred to the memory location, the processing is complete and the network adapter is at that point able to be configured for transferring the second element by prefetching (load) the next descriptor. Therefore, Golden implicitly discloses configuring and transferring being done concurrently).

As per claim 5, Golden discloses the method according to claim 1, wherein the loading comprises loading the packet descriptor into a fast descriptor queue for subsequent transfer to the communications adapter (paragraphs [0008, 0012, 0016], Golden teaches the computing device placing (loading) descriptors into multiple queues such as receive queues (fast descriptor queue). The network adapter fetches or pre-fetches the descriptors from the computing system's queue (fast descriptor queue).

As per claim 6, Golden discloses the method according to claim 5, further comprising loading a second packet descriptor into the fast descriptor queue, wherein the loading the second packet descriptor is performed prior to the transferring the second data element (paragraphs [0009, 0015], Golden teaches the computing device placing

(loading) descriptors into a queue (fast descriptor queue). The adapter pre-fetches (loads) another descriptor from the queue (fast descriptor queue) before the subsequent message (second data element) is received by the adapter for transfer).

As per claim 8, Golden discloses a computing node comprising:

- a fast data element transmitter for transferring a first data element and a second data element to a pre-defined destination (paragraphs [0009, 0010, 0013, 0015, 0019, 0045], Golden teaches writing (transferring) data (first data packet) from a received message to a specific memory location (destination). Golden teaches transferring the next incoming message (second data element) according to information contained in the pre-fetched descriptor. Subsequent packets (second data element) are sent to memory locations (destination) specified by the descriptor);
- a fast descriptor interface for loading a packet descriptor concurrently with the transferring of the first data element, wherein the packet descriptor identifies the pre-defined destination and is used to configure the fast data packet transmitter for transferring the second data element (paragraphs [0008-0010, 0017, 0019, 0045], Golden teaches placing (loading) descriptors in the network adapter's cache. The descriptors are used to identify the memory address to which data should be written. Golden teaches transferring the next incoming message (second data element) according to information contained in the pre-fetched descriptor. Subsequent packets (second data element) are sent to memory locations (destination) specified

by the descriptor. Transferring the packet and prefetching (loading) the next descriptor is done in this manner to reduce latency. Without waiting, the adapter is able to increase its rate of processing messages under conditions of heavy, bursty traffic. Once data is being transferred to the memory location, the processing is complete and the network adapter is at that point able to prefetch (load) the next descriptor. Therefore, Golden implicitly discloses loading and transferring being done concurrently).

As per claim 9, Golden discloses the computing node according to claim 8, further comprising a fast data queue for queuing data elements for transmission to the pre-defined destination (paragraphs [0004, 0006, 0033, 0037], Figure 2, According to Applicant's specification, an exemplary fast transmission queue structure has two queues: the fast data transmission queue and the fast descriptor queue. However, alternative embodiments operate with a single queue to queue entire data packets (pages 14-15). Golden teaches queue pair (QP) (fast data queue) having a send work queue and a receive work queue. Work requests having work elements (data elements) are placed in the appropriate queue. The receive queue comprise one or more descriptors indicating the memory location to which the data is to be written).

As per claim 11, Golden discloses the computing node according to claim 8, wherein the pre-defined destination is associated with a neighboring computer node (paragraphs [0003, 0006, 0008-0009], Golden teaches writing data to a destination computing device

(computer node) (also called a host). This device is coupled to (neighboring) the network adapter).

As per claim 12, Golden discloses the computing node according to claim 8, further comprising a fast descriptor queue for queuing the packet descriptor for subsequent transfer to the fast descriptor interface (paragraphs [0008, 0012, 0016], Golden teaches the computing device placing (loading) descriptors into multiple queues such as receive queues (fast descriptor queue). The network adapter fetches or pre-fetches the descriptors from the computing system's queue (fast descriptor queue).

As per claim 13, Golden discloses the computing node according to claim 12, further comprising loading a second packet descriptor into the fast descriptor queue prior to the transferring of the second data element (paragraphs [0009, 0015], Golden teaches the computing device placing (loading) descriptors into a queue (fast descriptor queue). The adapter pre-fetches (loads) another descriptor from the queue (fast descriptor queue) before the subsequent message (second data element) is received by the adapter for transfer).

As per claim 14, Golden discloses a signal bearing medium including a program which, when executed by a processor, performs operations for transferring a data message, the operations comprising:

- transferring a first data element to a pre-defined destination (paragraphs [0010, 0013, 0019, 0045], Golden teaches writing (transferring) data (first data packet) from a received message to a specific memory location (destination);
- loading a packet descriptor into a communications adapter, wherein the loading is concurrent with the transferring and the packet descriptor identifies the pre-defined destination (paragraphs [0008-0010, 0017, 0019, 0045], Golden teaches placing (loading) descriptors in the network adapter's cache. The descriptors are used to identify the memory address to which data should be written. The memory address corresponds to a memory location at a computing device. The adapter transfers the message data to the system memory location. The next descriptor is prefetched (loaded). Transferring the packet and prefetching (loading) the next descriptor is done in this manner to reduce latency. Without waiting, the adapter is able to increase its rate of processing messages under conditions of heavy, bursty traffic. Once data is being transferred to the memory location, the processing is complete and the network adapter is at that point able to prefetch (load) the next descriptor. Therefore, Golden implicitly discloses loading and transferring being done concurrently);
- transferring, in dependence upon the packet descriptor, a second data element to the pre-defined destination (paragraphs [0009, 0015, 0047, 0049], Golden teaches transferring the next incoming message (second data element) according to information contained in the pre-fetched descriptor. Subsequent packets (second

data element) are sent to memory locations (destination) specified by the descriptor).

As per claim 15, Golden discloses the signal bearing medium of claim 14, wherein the transferring of the first data element and the transferring of the second data element comprises loading the first data element and the second data element into a fast data queue, wherein the fast data queue only queues data elements for transmission to the pre-defined destination (paragraphs [0004, 0006, 0033, 0037], Figure 2, According to Applicant's specification, an exemplary fast transmission queue structure has two queues: the fast data transmission queue and the fast descriptor queue. However, alternative embodiments operate with a single queue to queue entire data packets (pages 14-15). Golden teaches queue pair (QP) (fast data queue) having a send work queue and a receive work queue. Work requests having work elements (data elements) are placed in the appropriate queue. The receive queue comprise one or more descriptors indicating the memory location to which the data is to be written).

As per claim 17, Golden discloses the signal bearing medium of claim 14, wherein the loading further comprises configuring, concurrently with the transferring of the first data element, the communications adapter for the transferring of the second data element (paragraphs [0008- 0049], According to Applicant's specification, pre-fetching causes the network adapter to pre-fetch the descriptor from the fast descriptor queue to begin configuration for transmission of the next data element (page 18). Golden teaches

fetching (loading) the next work item from the receive queue and writing (transferring) data to the location specified by the work item. Once these operations complete, the adapter can pre-fetch the next work item (descriptor) for the next message (element) that is received. This is configuration for transmission of the next data element. The next descriptor is prefetched (loaded). Transferring the packet and prefetching (loading) the next descriptor is done in this manner to reduce latency. Without waiting, the adapter is able to increase its rate of processing messages under conditions of heavy, bursty traffic. Once data is being transferred to the memory location, the processing is complete and the network adapter is at that point able to be configured for transferring the second element by prefetching (load) the next descriptor. Therefore, Golden implicitly discloses configuring and transferring being done concurrently).

As per claim 18, Golden discloses the signal bearing medium of claim 14, wherein the loading operation comprises loading the packet descriptor into a fast descriptor queue for subsequent transfer to the communications adapter (paragraphs [0008, 0012, 0016], Golden teaches the computing device placing (loading) descriptors into multiple queues such as receive queues (fast descriptor queue). The network adapter fetches or pre-fetches the descriptors from the computing system's queue (fast descriptor queue).

As per claim 19, Golden discloses the signal bearing medium of claim 18, wherein the operations further comprise loading a second packet descriptor into the fast descriptor queue, wherein the loading the second packet descriptor is performed prior to the

transferring the second data element (paragraphs [0009, 0015], Golden teaches the computing device placing (loading) descriptors into a queue (fast descriptor queue). The adapter pre-fetches (loads) another descriptor from the queue (fast descriptor queue) before the subsequent message (second data element) is received by the adapter for transfer).

15. Claims 3, 7, 10, 16, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goldenberg et al. (hereinafter "Golden", US Patent Publication 2004/0034718 A1) in view of Snyder et al. (hereinafter "Snyder", US Patent 5,522,039).

As per claim 3, Golden discloses the method according to claim 1.
Golden does not explicitly disclose wherein at least one of the first data element and the second data element each comprise a user data portion that is equal to the size of a cache buffer.
However, in an analogous art, Snyder teaches transferring actual network data to or from the network. The data packet contains a header portion (first element) of data and a user data portion (second element). The data passes from the system to an FDDI buffer or is loaded into an FDDI FIFO memory (cache buffer). The FIFO is a twenty-two word memory. Twenty-two words of data are loaded quickly into FIFO (cache buffer). The network adapter performs a checksum of the data being transferred (column 5, lines 22-34, 62-65, column 6, lines 7-10).

Therefore, one of ordinary skill in the art at the time the invention was made would have found it obvious to implement or incorporate Snyder's at least one of the first data element and the second data element each comprise a user data portion that is equal to the size of a cache buffer in Golden's method enabling the data to be channeled through the network at a desired speed without slowing down the system bus to execute additional transactions (Snyder, column 5, lines 35-37, 52-54).

As per claim 7, Golden discloses the method according to claim 5.
Golden does not explicitly disclose further comprising altering the packet descriptor while the packet descriptor is in the fast descriptor queue and reloading the packet descriptor into the communications adapter prior to transferring the second data element.
However, in an analogous art, Snyder teaches the processor giving the byte count and destination address (packet descriptor) of a first portion of a packet to the network adapter and control chip. The control chip stores this information in one of its two pairs of address and byte count registers (fast descriptor queue). The byte count (packet descriptor) may be adjusted (altered) to take advantage of bimodal distribution. This means that the number of packets to be transferred will vary and an optimum value will be selected based on characteristics of the computing device and the network. The control chip uses (reloads) the byte count (packet descriptor) to perform a checksum and direct the transfer of both the first and remaining portion of the data packet (column 6, lines 16-25, 31-33, 37-47, 54-61, column 7, lines 49-55, column 8, lines 13-19).

Therefore, one of ordinary skill in the art at the time the invention was made would have found it obvious to implement or incorporate Snyder's altering the packet descriptor while the packet descriptor is in the fast descriptor queue and reloading the packet descriptor into the communications adapter prior to transferring the second data element in Golden's method in order to take advantage of the bimodal distribution wherein selection of an optimum value of byte count for data transfer is performed (Snyder, column 6, lines 39-40, 46-48).

As per claim 10, Golden discloses the computing node according to claim 8.
Golden does not explicitly disclose wherein at least one of the first data element and the second data element each comprise a user data portion that is equal to the size of a cache buffer.
However, in an analogous art, Snyder teaches transferring actual network data to or from the network. The data packet contains a header portion (first element) of data and a user data portion (second element). The data passes from the system to an FDDI buffer or is loaded into an FDDI FIFO memory (cache buffer). The FIFO is a twenty-two word memory. Twenty-two words of data are loaded quickly into FIFO (cache buffer). The network adapter performs a checksum of the data being transferred (column 5, lines 22-34, 62-65, column 6, lines 7-10).

Therefore, one of ordinary skill in the art at the time the invention was made would have found it obvious to implement or incorporate Snyder's at least one of the first data element and the second data element each comprise a user data portion that

is equal to the size of a cache buffer in Golden's computing node enabling the data to be channeled through the network at a desired speed without slowing down the system bus to execute additional transactions (Snyder, column 5, lines 35-37, 52-54).

As per claim 16, Golden discloses the signal bearing medium of claim 14.
Golden does not explicitly disclose wherein each of at least one of the first data element and the second data element comprises a user data portion that is equal to the size of a cache buffer.
However, in an analogous art, Snyder teaches transferring actual network data to or from the network. The data packet contains a header portion (first element) of data and a user data portion (second element). The data passes from the system to an FDDI buffer or is loaded into an FDDI FIFO memory (cache buffer). The FIFO is a twenty-two word memory. Twenty-two words of data are loaded quickly into FIFO (cache buffer). The network adapter performs a checksum of the data being transferred (column 5, lines 22-34, 62-65, column 6, lines 7-10).

Therefore, one of ordinary skill in the art at the time the invention was made would have found it obvious to implement or incorporate Snyder's at least one of the first data element and the second data element each comprise a user data portion that is equal to the size of a cache buffer in Golden's medium enabling the data to be channeled through the network at a desired speed without slowing down the system bus to execute additional transactions (Snyder, column 5, lines 35-37, 52-54).

As per claim 20, Golden discloses the signal bearing medium of claim 18.

Golden does not explicitly disclose wherein the operations further comprise altering the packet descriptor while the packet descriptor is in the fast descriptor queue and reloading the packet descriptor into the communications adapter prior to transferring the second data element.

However, in an analogous art, Snyder teaches the processor giving the byte count and destination address (packet descriptor) of a first portion of a packet to the network adapter and control chip. The control chip stores this information in one of its two pairs of address and byte count registers (fast descriptor queue). The byte count (packet descriptor) may be adjusted (altered) to take advantage of bimodal distribution. This means that the number of packets to be transferred will vary and an optimum value will be selected based on characteristics of the computing device and the network. The control chip uses (reloads) the byte count (packet descriptor) to perform a checksum and direct the transfer of both the first and remaining portion of the data packet (column 6, lines 16-25, 31-33, 37-47, 54-61, column 7, lines 49-55, column 8, lines 13-19).

Therefore, one of ordinary skill in the art at the time the invention was made would have found it obvious to implement or incorporate Snyder's altering the packet descriptor while the packet descriptor is in the fast descriptor queue and reloading the packet descriptor into the communications adapter prior to transferring the second data element in Golden's medium in order to take advantage of the bimodal distribution wherein selection of an optimum value of byte count for data transfer is performed (Snyder, column 6, lines 39-40, 46-48).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barbara N. Burgess whose telephone number is (571) 272-3996. The examiner can normally be reached on M-F (8:00am-4:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Ettinene can be reached on (571) 272-4001. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Barbara N Burgess
Examiner
Art Unit 2157

October 14, 2007